

MIDDLE EAST TECHNICAL UNIVERSITY

DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

EE 463 - Static Power Conversion II - Term Project

Simulation Report

Doge Power Inc.

12V - 100W Isolated DC-DC Converter

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Onur Öztaş .....

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# Introduction

# Topology Selection

In this project 100W isolated dc-dc converter design is required. In the below, the project specifications are listed as follows:

* Minimum input voltage : 220V
* Maximum input voltage : 400V
* Output voltage : 12V
* Output Power : 100W
* Output voltage peak-peak ripple : 4%
* Line regulation : 3%
* Load regulation : 3%

For the design of such a system, first a suitable topology selection is required. Since the system should be an isolated system, the following topology alternatives can be chosen as follows:

* Flyback Converter
* Forward Converter
* Push – Push Converter
* Half Bridge
* Full Bridge

*Flyback Converter:*

Advantages of this converter are:

* No output inductance requirement
* Ability to supply multiple output voltages
* Less component requirement compared to the other converters

Disadvantages of this converter are:

* Closed loop bandwidth in CCM operation is narrow
* Large output capacitor requirement

Since our input margin is too large, this converter may not give good results in our conditions. Also, it is power ratings are top limit for our specifications. That may result in higher duty cycle requirement. For those reasons, this converter didn’t selected.

*Forward Converter:*

Advantages of this converter are:

* Drive circuit is simpler compared to other topologies
* One switching transistor is required

Disadvantages of this converter are:

* Transformer utilization is not sufficient compared to the push pull and bridge topologies. Dmax is limited by 50%.
* Blocking voltage of the transistors are 2 times of the input voltage. That increases ratings of the component.
* It may go into DCM operation

In our design purposes, increasing transformer utilization is critical. Since this topology uses transformer insufficiently, it is not preferred in our design.

*Half Bridge:*

This topology presents best transformer utilization. It provides low cost and small space. However, when controller research is conducted, it is realized that the analog controllers for this topology is not applicable. Most of the controller stabilizes output voltage with respect to reference value. However, the input capacitance middle point is discarded almost all of the controllers. Therefore, due to the insufficient integrated circuits for this topology, it is not selected.

*Full Bridge:*

This topology generally preferred in larger than 500W applications. It has 4 transistors in the primary side of the topology. Since the input voltage level of this project is around 200-400V margin, selecting 4 transistors at those ratings will brings a lot of project costs. Therefore, for that reason this topology is discarded.

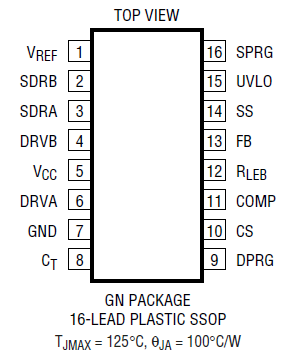
*Push – Pull Converter:*

This topology uses 2 input switch and 2 output diode. Moreover, additional LC filter to the output is required. Since its transformer utilization is good, the required transformer core size is relatively small compared to others, and transformer ratings are smaller compared to the Forward. Also, its filter requirement is small compared to the Flyback and Forward topologies. It is one the biggest disadvantage is central top transformer structure. However, while considering the other advantages this converter has more useful for this project. Therefore, this one is selected as a SPMS design application.

# Controller Design

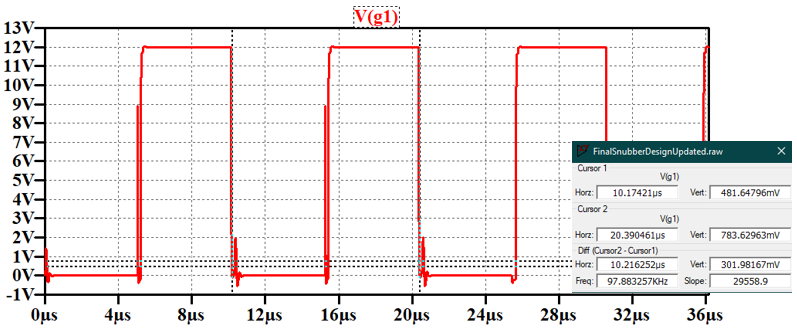
In this project, stable output is desired whereas input is changing from 220V to 400V. That yields a controller requirement. For this purpose, LT3723-1 current mode controller is selected as it will be expressed in component selection section. This controller can act both as controller and as gate driver for the MOSFETs. Therefore, it decreases the component requirement to a single component. However, the biggest drawback of this controller is that it does not satisfy the isolation criteria of the project. Therefore, in addition to this integrated circuit (IC) an opto coupler and opto coupler driver IC’s is selected, which completes the isolation problem of this design. For opto-coupler MOC207M is selected, for its driver LT1431 IC is selected.

In designing controller, first the main IC should be programmed such that it suits in this application. For step by step improvement, the pin configuration and package information of this IC can be seen in Figure X.



This project is designed with 100 kHz operating frequency. Selecting operating frequency high decreases, the size of the magnetic components and output filter components. However, while frequency increases the switching losses also increases. Therefore, that will yield less efficiency. Finding optimum point is crucial. For that purpose, 100kHz operating frequency is selected. In order to program IC to 100 kHz frequency, its CT pin is used. The following formula programs the operating frequency of the IC by connecting capacitor from that pin to ground.

After inserting this capacitor, the frequency of the gate signals is measured as in Figure X.



Selecting capacitor value in large significant figures arranges the frequency exactly to the 100kHz. However, in practice it is not practical. Therefore, this amount is decided enough for this application.

In push pull topology, gates of the both MOSFETs are off during some time. That time is known as dead time. Dead time of this IC is programmed with connecting resistances to the SPRG and DPRG pins. The values are determined from the data sheet dead time plot. It is selected as higher as so that it suits in our application. They are selected as 250kΩ. That is enough to stabilize output in the 12V reference level.

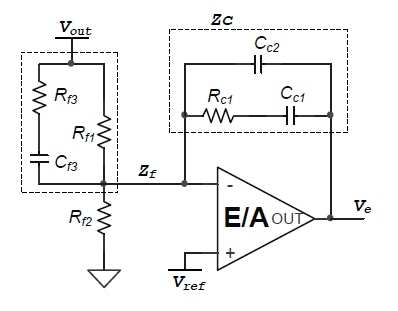
Controllers provides controlled output by some external circuits constructed to the control pins. These circuits are known as ‘Compensator Circuits’. Since the control loop in this project is completed by using the opto-coupler circuits, the compensation circuits are constructed in the opto-coupler driver circuit pins. Also, feedback from the output is taken by the opto-coupler driver. Therefore, the feedback pin of the controller is connected to ground. It continuously provides output while compensation signal is provided. In the next subsection the compensator circuit design is explained in detail.

# Compensator Circuit Design

The input voltage range in this application is quite large. Therefore, compensator circuit performance is crucial in order to stabilize output to 12V. There are 3 main compensator types, which are:

* Type I compensator
* Type II compensator
* Type III compensator

Type I is used for basic application. In SMPS designs, type II compensator is preferred generally. However, in large range application that may not be sufficient. In that cases, Type 3 compensator can be used. Since this project conducts in wide range input voltages, it is required to use type 3 compensator. In type 3 design, the following reference circuit configuration is referred.



In the design of these components, first pole zero locations are determined. For that purpose, the LC frequency of the output filter is calculated as:

And, ESR frequency of the capacitor is calculated as:

The pole-zero locations are selected by these frequencies accordingly as follows:

Finally, these is a single pole at the origin, which is

The circuit components based on these formulas are calculated from the following formulas based on taking some suitable value, which can be 2.2nF as a good start. If not worked, it can be updated.

In here, the voltage is the oscillation voltage of the IC. It is 2.35V from datasheet.

These are the general formulas used in the design. However, finding values from these formulas generally not sufficient at first. It required fine tuning algorithms. Calculating again and again from at first step is a messy work. Therefore, as can be seen in Appendix A, a MATLAB m file is prepared.

When the first values are taken, they are simulated. They will stabilize at 12V output in both 220V and 400V input values. However, the final waveform of output voltage at steady state is not sufficient. It is oscillating very high. In order to solve this problem, the transfer function of the compensator circuit is extracted and written into the m file. Then, by plotting bode diagram of that transfer function, the effect of each component indicated above is observed one by one. It is crucial to obtain phase margin larger than 40 degrees. At first, it is around 40 degrees, and as said it is not good for output voltage stabilization. While observing each element effect to the bode plot, it is realized that increasing third pole frequency increases the phase margin of the system, and improves stability also. At final step third pole frequency is selected as:

It results in -108 degrees phase at 100kHz frequency. It is phase margin is found as:

The resulted phase margin is excellent for design. Its results are also very good both in terms of transient and in terms of steady state.

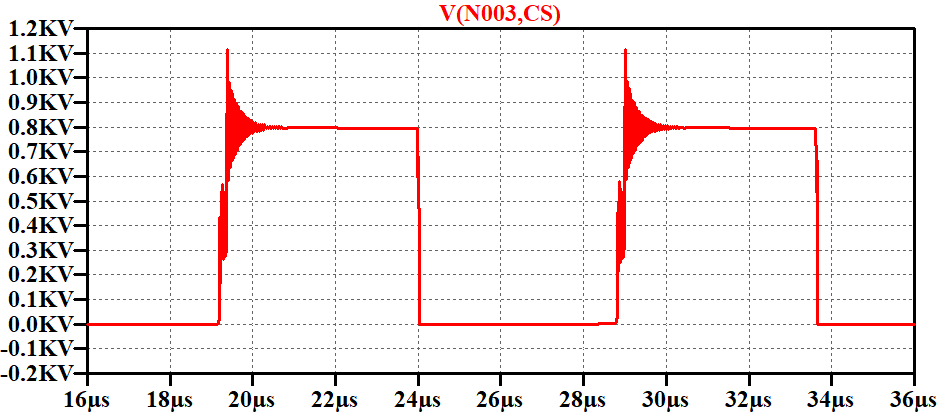
# Snubber Circuit Design

In most of the industrial applications, designing circuits with low electromagnetic interference (EMI) is required. The reason for that is designing parts of a project in separately is not affected from this phenomenon because it has an effect to the neighboring components. They usually distort their operating frequencies and also operating performances. Higher EMI problems at some point also distort the operation performance of the product also. Therefore, suppressing those EMI spikes is critical. For that purpose, snubber circuits are preferred. There are 3 types of mostly used snubber circuit configurations. These can be order as:

* C snubber
* RC snubber
* R//D -C snubber

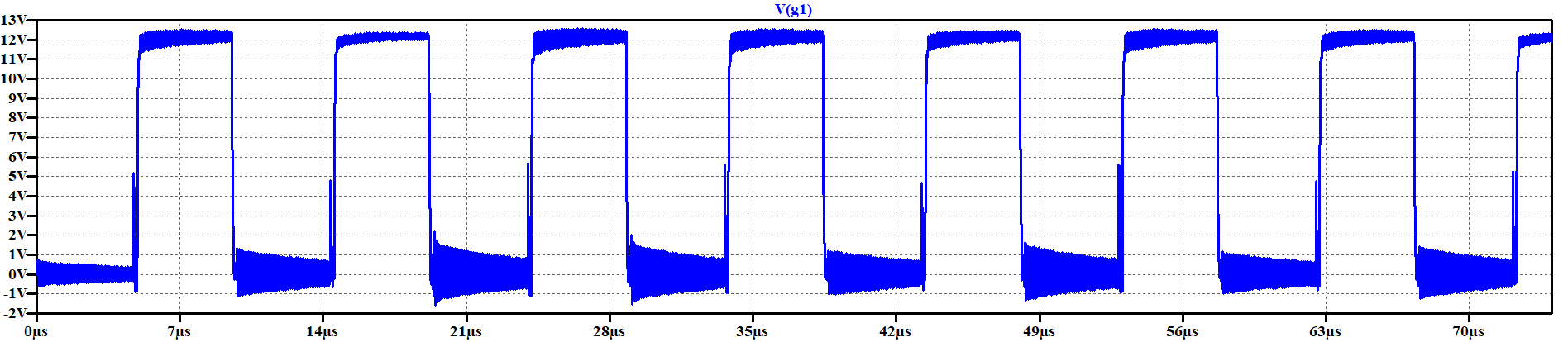
Inserting only C snubbers, decreases system operating speed. When system slows down, then it increases EMI radiation, which is also called ringings. To eliminate ringing R is inserted. In RC snubber that ringing also canceled. Therefore, it yields best result. In another application, resistor is parallel with diode and connected to capacitor in series. The purpose for this application decreasing resistive losses exists in the system. However, since this application works under 100kHz switching frequency, diode’s switching losses are quite high. Also, the cost of the diodes will increase project costs. For that reasons, R-C snubber circuits are used.

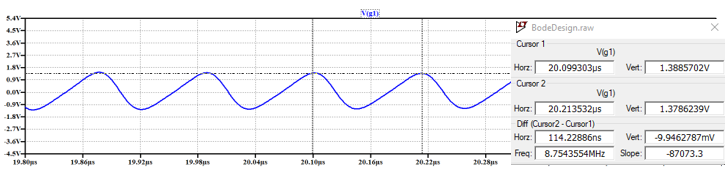
Before starting the snubber circuit design, the drain-to-source voltage of MOSFET is observed as in Figure X.



The effect of EMI radiations can be observed easily in this figure. Therefore, eliminating this is critical for SMPS design.

In the design of the snubber circuits, there is a guideline for the push-pull topology. Accordingly, first the resonance frequency of the spikes is measured as shown in Figure X.





Resonant frequency is measured as 8.75 MHz Insert parallel capacitor to the MOSFET’s drain to source legs so that that frequency drops half of it. The value of the inserted capacitor is 1100 pF that reduces spike frequency by a factor of two. That capacitance is the three times the value of the parasitic capacitance that created voltage spikes.

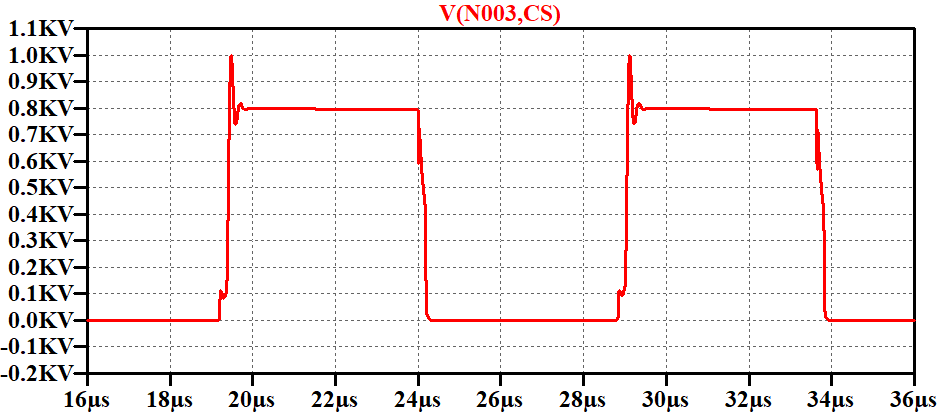
By using this value and the resonant frequency measured as above, the value of the parasitic inductance can be found as below.

From these two found values, the characteristics impedance of the resonance can be found as below.

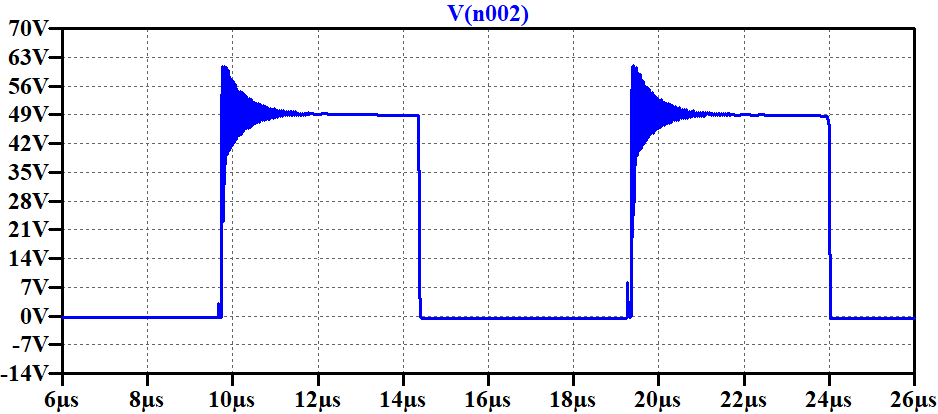
From the calculated impedance and capacitor values, the RC snubber circuits component values can be chosen as;

While selecting the snubber capacitance value in found range, the gate signals waveforms observed as insufficient form when is 400V. Therefore, in order to fix that problem snubber capacitor for MOSFET is selected as 500pF. It is decided with trial and error way around the found range. It is decided around 3 trial. Therefore, final selected values are:

After inserting snubber components the drain-to-source voltage of the MOSFET’s is observed as in Figure X.



For diode, the same problem is existing. It is voltage waveform can be observed before inserting snubber circuits as in Figure X.



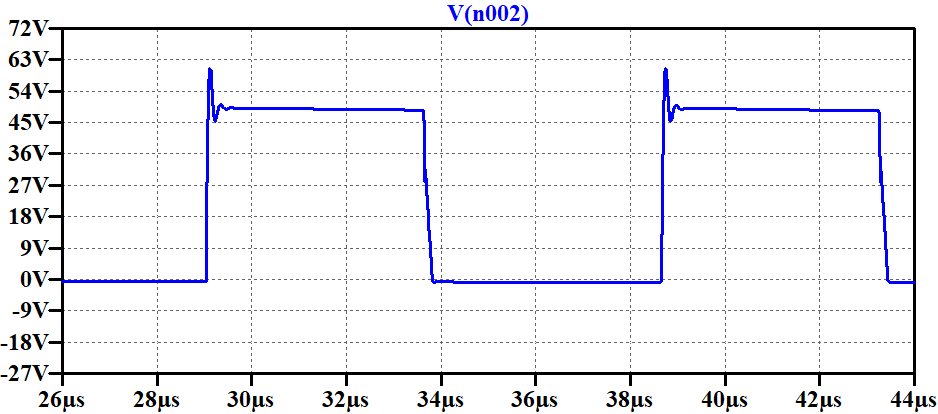
The same procedure applied to the MOSFET’s can be applied for this component also. First resonance frequency of the spike is measured. It is found as 224 MHz Then, by connecting shunt capacitor the value of the parasitic capacitance is found in which the resonance frequency is reduced by a factor of two. Finally, by using the capacitance and resonance frequency values, inductance and reactance values can be found. At the end, almost same of the reactance is selected as snubber resistance, and 200pF capacitance value is selected as the snubber capacitance.

Capacitance value that reduces spike resonance frequency by half is 100pF. Then, the parasitic capacitance is:

At this point, similar to the MOSFET design, resistor value is selected as found impedance value, and capacitor is selected as:

Selected exact values are:

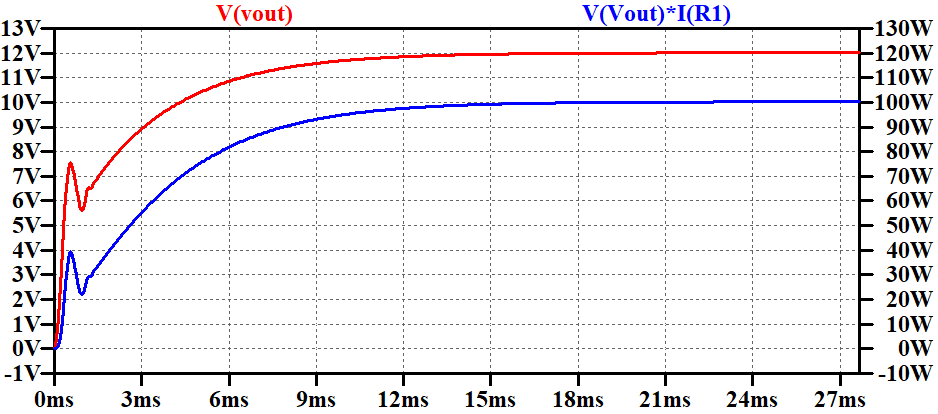
After inserting snubber components, diode voltage waveform is observed as in Figure X.



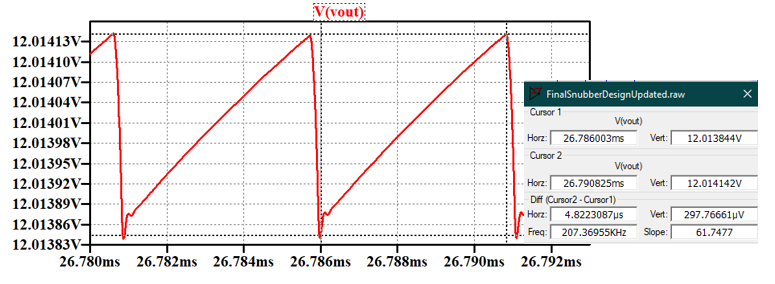
# Component Selection

# Simulation Results

When input voltage is 220V, the output voltage and power waveform is as shown in Figure X.

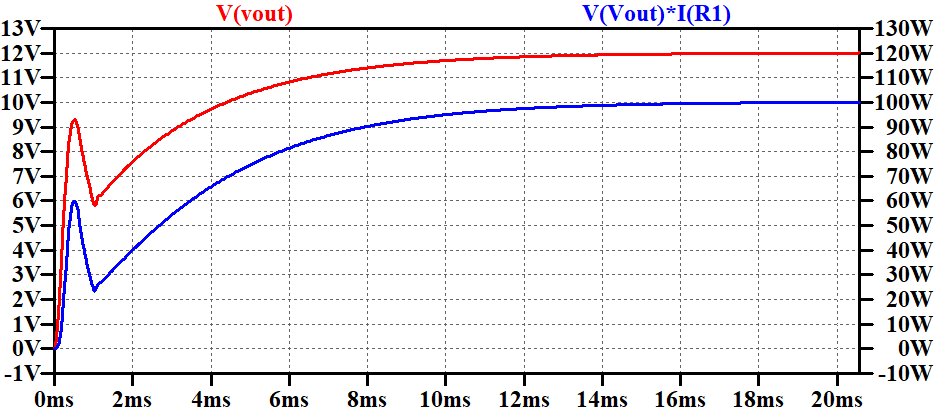


Output voltage stabilizes at 12.02V. The output voltage ripple can be seen in Figure X.



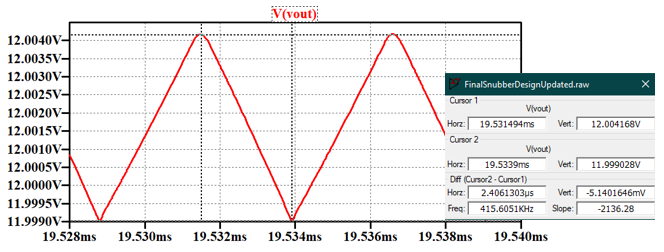
From no load to full load the output voltage waveform can be seen in Figure X.

When input voltage is 400V, the output voltage and power waveform is as shown in Figure X.



The output voltage stabilizes at 12.0014V.

The output voltage ripple can be seen in Figure



From no load to full load the output voltage waveform can be seen in Figure X.

The line regulation when input voltage changes from 220 V to 400 V can be calculated from the above results as:

# Conclusion

# Appendix

%Doge Power Compensator Design File

L = 80e-6; %Output Inductance

C = 330e-6; %Output Capacitance

ESR = 56e-3; %Capacitor ESR value

F\_lc = 1/(2\*pi\*sqrt(L\*C)); %Filter frequency

F\_esr = 1/(2\*pi\*ESR\*C); %ESR frequency

Fsw = 100e3; %Switching frequency

Fzero = Fsw/10; %Center frequency

Vref = 2.5; %Driver reference voltage

Vout = 12; %Output voltage

Vosc = 2.35; %Peak-to-Peak oscillator amplitude voltage

Vin = 300; %Minimum input voltage

%Type 3 Compensator pole and zero frequencies

Fz2 = F\_lc; %Second zero frequency

Fz1 = 0.75\*F\_lc; %First zero frequency

Fp2 = F\_esr\*10; %Second pole frequency

%Fp3 = Fsw/2; %Third pole frequency

Fp3 = Fsw\*2.25; %Third pole frequency

%Type 3 Compansator Parameters

Cf3 = 2.2e-9; %Cf3 is selected then rest is calculated from it

Rf3 = 1/(2\*pi\*Cf3\*Fp2); %Voltage division compensator Rf1 = 1/(2\*pi\*Cf3\*Fz2)-Rf3; %Voltage division top resistor Rf2 = (Rf1\*Vref)/(Vout-Vref); %Voltage division bottom

resistor

Rc1 = (2\*pi\*Fzero\*L\*C\*Vosc)/(Vin\*Cf3); Cc1 = 1/(2\*pi\*Rc1\*Fz1);

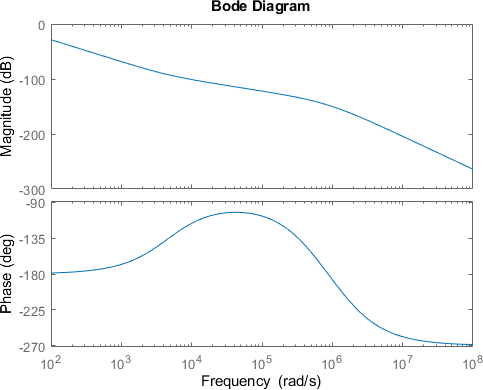
Cc2 = 1/(2\*pi\*Rc1\*Fp3);

%Type 3 Compensator Transfer Function s = tf('s');

H = tf([(Rc1\*Cc1+Rc1\*Cc1\*Cf3\*(Rf1+Rf3)) (1+Cf3\*(Rf1+Rf3))], [(Cc2\*Rc1\*Cf3\*Rf3\*Cc1\*Rf1) (Cc1\*Rf1\*Rc1\*Cc2+Cc1\*Rf1\*Rf3\*Cf3) (Cc1\*Rf1)

0 0]);

bode(H);



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